

Docket No.: 071971-0015

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277  
Shiro SAKIYAMA, et al. : Confirmation Number: CNF NO. 6689  
Application No.: 10/511,165 : Group Art Unit: 2811  
Filed: October 14, 2004 : Examiner: Not yet assigned  
For: SEMICONDUCTOR INTEGRATED CIRCUIT

**REQUEST FOR CORRECTED FILING RECEIPT**

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Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that the Domestic priority data is incorrect. Attached is a copy of the Front Page of the Published International Application, which evidences that the Domestic Priority data should read: PCT/JP04/01942 02/19/2004. It is requested that a corrected filing receipt be issued.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty  
Registration No. 36,139

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
Phone: 202.756.8000 MEF:blg  
Facsimile: 202.756.8087  
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CONFIRMATION NO. 6689

20277  
 MCDERMOTT WILL & EMERY LLP  
 600 13TH STREET, N.W.  
 WASHINGTON, DC 20005-3096

## FILING RECEIPT



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Date Mailed: 04/08/2005

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## Applicant(s)

Shiro Sakiyama, Yawata-shi, Kyoto, JAPAN;  
 Masayoshi Kinoshita, Settsu-shi, JAPAN;  
 Masaya Sumita, Amagasaki-shi, JAPAN;

**Power of Attorney:** The patent practitioners associated with Customer Number 20277.

## Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/01942 02/19/2003

## Foreign Applications

JAPAN 2003-047418 02/25/2003

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**Early Publication Request:** No

## Title

Semiconductor integrated circuit

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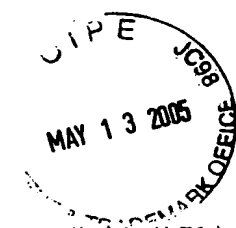
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(71) 出願人 (米国を除く全ての指定国について): 松下電  
器産業株式会社 (MATSUSHITA ELECTRIC INDUS-  
TRIAL CO., LTD.) [JP/JP]; 〒5718501 大阪府門真市大  
字門真 1 0 0 6 番地 Osaka (JP).  
(72) 発明者; および  
(75) 発明者/出願人 (米国についてのみ): 崎山 史  
朗 (SAKIYAMA, Shiro). 木下 雅善 (KINOSHITA,  
Masayoshi). 炭田 昌哉 (SUMITA, Masaya).

(74) 代理人: 前田 弘, 外 (MAEDA, Hiroshi et al.); 〒  
5500004 大阪府大阪市西区鞠本町 1 丁目 4 番 8 号  
本町中島ビル Osaka (JP).

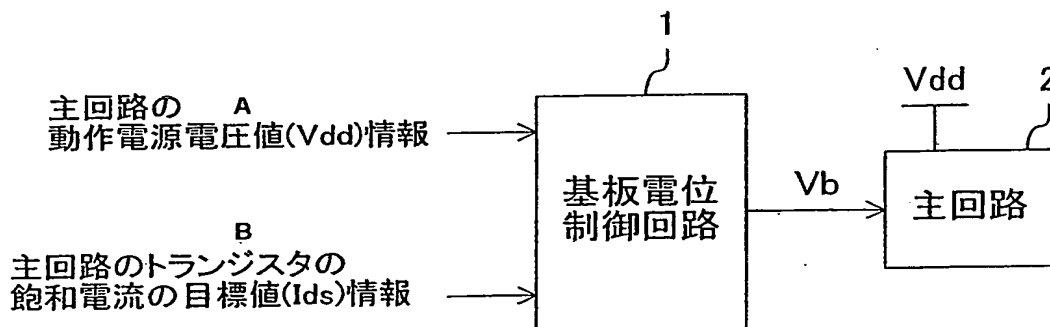
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(54) Title: SEMICONDUCTOR INTEGRATED CIRCUIT

(54) 発明の名称: 半導体集積回路



A...INFORMATION CONCERNING OPERATING POWER  
SUPPLY VOLTAGE (Vdd) OF MAIN CIRCUIT  
B...INFORMATION CONCERNING TARGET SATURATION  
CURRENT VALUE (IdS) OF TRANSISTOR OF MAIN CIRCUIT  
1...SUBSTRATE POTENTIAL CONTROLLING CIRCUIT  
2...MAIN CIRCUIT

(57) Abstract: A semiconductor integrated circuit comprises a main circuit (2) which is composed of a MOS transistor wherein a source and a substrate are separated from each other. A substrate potential controlling circuit (1) controls the substrate potential of the MOS transistor of the main circuit (2) so that the actual saturation current value of the MOS transistor which constitutes the main circuit (2) becomes equal to a target saturation current value (IdS) of the main circuit (2) at the operating power supply voltage (Vdd). Consequently, even when the operating power supply voltage of the semiconductor integrated circuit is lowered, variations in the operating speed can be suppressed within a small range.

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MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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添付公開書類:

— 国際調査報告書

(57) 要約: 半導体集積回路において、主回路2は、ソースと基板とが分離されたMOSトランジスタで構成される。基板電位制御回路1は、主回路2を構成するMOSトランジスタの実際飽和電流値が、主回路2の動作電源電圧 $V_{dd}$ の下での目標飽和電流値 $I_{ds}$ となるように、主回路2のMOSトランジスタの基板電位を制御する。従って、半導体集積回路の動作電源電圧が低電圧化しても、動作速度のばらつきを小さく抑制できる。